REMARKS

Applicants appreciate the Examiner's thorough examination of the present application as evidenced by the Office Action of December 19, 2005 (hereinafter "Office Action"). Applicants especially appreciate the indication that Claim 26 recites patentable subject matter and the allowance of Claims 34, 35, and 37. In response, Applicants respectfully submit that the cited references do not disclose or suggest, at least, the recitations of the pending independent claims. Accordingly, Applicants submit that all pending claims are in condition for allowance. Favorable reconsideration of all pending claims is respectfully requested for at least the reasons discussed hereafter.

Independent Claims 1, 14, and 43 are Patentable

Independent Claims 1, 14, and 43 stand rejected under 35 U.S.C. §103(a) as being unpatentable over U. S. Patent No. 6,438,670 to McClannahan (hereinafter "McClannahan") in view of U. S. Patent No. 6,101,197 to Keeth et al. (hereinafter "Keeth"). Independent Claim 1 is directed to a memory device controlled by a memory controller and recites, in part:

> A semiconductor memory device controlled by a memory controller, comprising:
> a delay control register for receiving delay control information from the memory controller and storing the received delay control information; and
> ...(Emphasis added)

Thus, according to independent Claim 1, delay control information is received from the memory controller and stored in a delay control register at the memory device. Claims 14 and 43 include similar recitations. For example, Claim 14 is directed to a method for controlling the delay time of an input signal input to a semiconductor memory device and includes the recitation:

> receiving delay control information from the memory controller and storing the received delay control information;

Claim 43 includes the recitation:

> receiving delay control information from the memory controller at the memory device;

Applicants respectfully submit that McClannahan does not disclose or suggest receiving delay control information from a memory controller at a memory device as recited in Claims 1, 14, and 43. In fact, the Office Action acknowledges that "McClannahan does not explicitly disclose a delay control register for receiving delay control information from the memory controller." (Office Action, page 4). The Office Action alleges, however, that the delay control register 204 of FIG. 4 of Keeth provides the missing teaching. (Office Action, pages 4 and 5). Applicants respectfully disagree with this interpretation of FIG. 4 of Keeth. In sharp contrast with the recitations of independent Claims 1, 14, and 43 that state that the delay control information is received and/or stored at a memory device that is controlled and/or communicatively coupled to a memory controller, the storage register 204 of Keeth is part of the array control circuit 182 shown in FIGS. 3 and 4. Applicants can find no teaching or suggestion in Keeth that the memory array 180 shown in FIG. 3 of Keeth can receive and/or store delay control information.

Accordingly, for at least the foregoing reasons, Applicants respectfully submit that independent Claims 1, 14, and 43 are patentable over McClannahan and Ryan, either alone or in combination, and that Claims 2 - 13, 15, and 44 are patentable at least per the patentability of independent Claims 1, 14, and 43.

Independent Claims 3, 8, 16, 20, and 24 are Patentable

Independent Claims 3 and 8 stand rejected under 35 U.S.C. §102(e) as being anticipated by McClannahan. Independent Claims 16, 20, and 24 stand rejected under 35 U.S.C. §103(a) as being unpatentable over McClannahan in view of Keeth. Independent Claim 3 is directed to a memory controller for controlling memory modules and recites, in part:

> ...
>
> a delay control register for receiving delay control information according to a specification from serial presence detectors (SPD) loaded into the memory modules and storing the received delay control information; and
>
> ...

Thus, according to independent Claim 3, the memory controller comprises a delay control register that receives delay control information from one or more memory modules. The

delay control information is stored in SPDs that are loaded into the memory modules. Claims 8, 16, 20, and 24 include similar recitations. For example, independent Claim 24 recites, in part:

> a plurality of memory modules, a respective one of which being responsive to a control signal and having delay control information stored thereon; and
>
> ...

Thus, according to independent Claim 24, delay control information is stored on one or more of the plurality of memory modules.

The Office Action appears to acknowledge that McClannahan does not disclose a delay control register for receiving delay control information according to a specification from serial presence detectors (SPD) loaded into the memory modules (Office Action, page 3), but page 2 of the Office Action alleges that this is disclosed in FIG. 1, col. 6, lines 8 - 13, and col. 8, lines 38 - 51 of McClannahan.

Applicants respectfully disagree as FIG. 1 of McClannahan is directed to a memory controller 10, not memory modules as recited in Claims 3, 8, 16, 20, and 24. Thus, the configuration register 26 shown in FIG. 1 as part of a tuning circuit 22 is part of a memory controller 10, not a memory module.

The passage of McClannahan at col. 8, lines 38 - 51 merely explains that the memory storage devices 76 have timing parameters that are associated therewith. This passage does not disclose or suggest that the memory storage devices 76 include serial presence detectors loaded therein that contain delay control information. Rather, McClannahan's text explains that "[t]he counting parameters and interface logic necessary for controlling the data transfer with such devices are generally known in the art." (McClannahan, col. 8, lines 49 - 51). Thus, the timing parameters for such conventional storage devices are generally known allowing one skilled in the art to design the interface logic necessary for controlling data transfer to and from these storage devices.

With respect to independent Claims 16, 20, and 24, these claims stand rejected based on the combination of McClannahan and Keeth. As discussed above, McClannahan fails to disclose or suggest storing delay control information on memory modules using, for example,

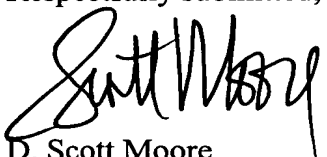
SPDs. In rejecting Claims 16, 20, and 24, the office Action does not include any additional analysis or point to any portions of Keeth that are alleged to disclose or suggest, at least, these teachings that are missing from McClannahan. (Office Action, page 6). Moreover, Applicants submit that Keeth appears to contain no disclosure or suggestion related to storing delay control information on the memory array 180 shown in FIG. 3.

Accordingly, for at least the foregoing reasons, Applicants respectfully submit that independent Claims 3, 8, 16, 20, and 24 are patentable over McClannahan and Keeth, either alone or in combination, and that Claims 4 - 7, 9 - 13, 17 - 19, 21 - 23, and 25 - 30 are patentable at least per the patentability of independent Claims 3, 8, 16, 20, and 24.

CONCLUSION

In light of the above amendments and remarks, Applicants respectfully submit that the above-entitled application is now in condition for allowance. Favorable reconsideration of this application, as amended, is respectfully requested. If, in the opinion of the Examiner, a telephonic conference would expedite the examination of this matter, the Examiner is invited to call the undersigned attorney at (919) 854-1400.

Respectfully submitted,



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CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited with the United States Postal Service as first-class mail in an envelope addressed to: Mail Stop Amendment, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450 on June 16, 2006.

Candi L. Riggs